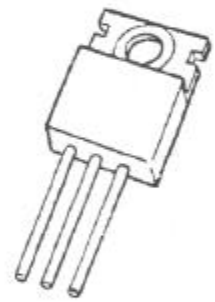
SCR

C122

8 A RMS Up to 600 Volts

The C122 is a molded silicon plastic SCR which incorporates General Electric's new POWER-GLAS glassivation process. This process provides for an intimate void-free bond between the silicon chip and the glass coating significantly improving performance and reliability.



JEDEC TO-220AB

FEATURES:

- Glassivated silicon chip for maximum reliability in AC or DC circuitry
- No maximum torque limit on mounting screw
- Round leads – greatly simplifies customer assembly
- Six standard lead forming configurations available from factory (including TO-66 compatibility)
- Special selections for non-standard gate requirements available upon request

TYPICAL SCR APPLICATIONS

	GENERAL FUNCTIONS				
Application	Motor Control	Temperature Control	Relay & Solenoid Driver	Power Regulator	Capacitor Discharge Circuit
Process Control Equipment	X	X	X	X	
Reproduction Equipment		X	X	X	
Blender, Mixers	X				
Hand Tools	X				
Machine Tools/Misc. Mfg.	X		X		
Sewing Machines	X				
Laundry			X		X
Farm Equipment	X		X		X
Photographic Equipment	X	X			
Clutches/Brakes			X		
Industrial Timers			X		
Vending Machines	X	X	X		
Battery Chargers				X	
Business Machines	X		X	X	
Gas & Oil Ignitors			X		X
Internal Combustion Engine Ignitions					X

MAXIMUM ALLOWABLE RATINGS

Type	Repetitive Peak Off-State Voltage, V_{DRM}(3) T_C = -40°C to +100°C	Repetitive Peak Reverse Voltage, V_{RRM}(1)(3) T_C = -40°C to +100°C	Non-Repetitive Peak Reverse Voltage, V_{RSM}(1)(2) T_C = -40°C to +100°C
C122F	50 Volts	50 Volts	75 Volts
C122A	100 Volts	100 Volts	200 Volts
C122B	200 Volts	200 Volts	300 Volts
C122C	300 Volts	300 Volts	400 Volts
C122D	400 Volts	400 Volts	500 Volts
C122E	500 Volts	500 Volts	600 Volts
C122M	600 Volts	600 Volts	700 Volts

Peak positive anode voltage (T_C = -40°C to +100°C) . . . . . 560 Volts
RMS On-State Current, $I_{T(RMS)}$ . . . . . 8 Amperes (all conduction angles)
Average On-State Current, $I_{T(AV)}$ . . . . . Depends on conduction angle (See Charts 3 and 4)
Critical Rate-Of-Rise of On-State Current, di/dt: (4)
Gate triggered operation . . . . . (see Chart 10)
Switching from 200 volts . . . . . 100 Amperes per microsecond
Switching from 500 volts . . . . . 50 Amperes per microsecond
Peak One Cycle Surge (non-rep) On-State Current, I_{TSM} 50 Hz . . . . . 82 Amperes
60 Hz . . . . . 90 Amperes
I^2t (for fusing), for times at 8.3 milliseconds . . . . . } see Chart 12 } . . . . . 34 Ampere^2 seconds
1.5 milliseconds . . . . . } see Chart 12 } . . . . . 27 Ampere^2 seconds
Peak Gate Power Dissipation, P_{GM} . . . . . 5 Watts for 10 microseconds (see Chart 6)
Average Gate Power Dissipation, $P_{G(AV)}$ . . . . . 0.5 Watts
Peak Positive Gate Current I_{GM} . . . . . see Chart 6
Peak Positive Gate Voltage, V_{GM} . . . . . see Chart 6
Peak Negative Gate Voltage, V_{GM} . . . . . 5 Volts
Storage Temperature, T_{stg} . . . . . -40°C to +125°C
Operating Temperature, T_J . . . . . -40°C to +100°C

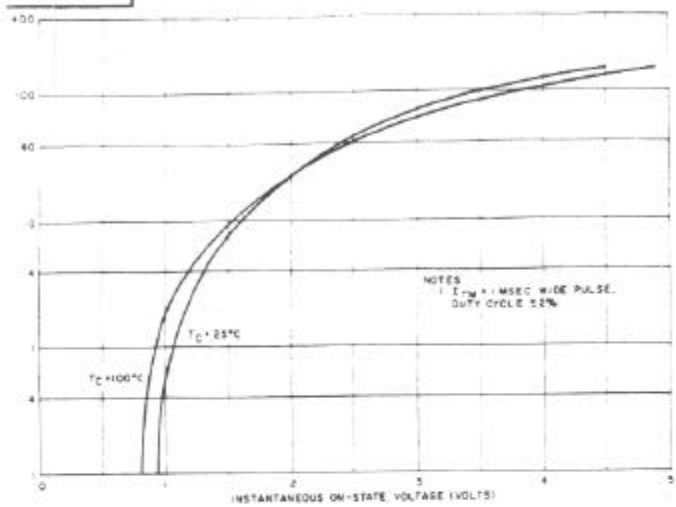
NOTES:

1. Values apply for zero or negative gate voltage only.
2. Half sine wave voltage pulse, 10 millisecond duration.
3. During performance of the off-state and reverse blocking tests, the thyristor should not be tested with a constant source which would permit applied voltage to exceed the device rating.
4. di/dt rating is established in accordance with JEDEC Suggested Standard No. 7, Section 5.1.2.4, Off-state (blocking) voltage capability may be temporarily lost immediately after each current pulse for duration less than the period of the applied pulse repetition rate. The pulse repetition rate for this test is 400 Hz. The duration of the JEDEC di/dt test condition is 5.0 seconds (minimum).

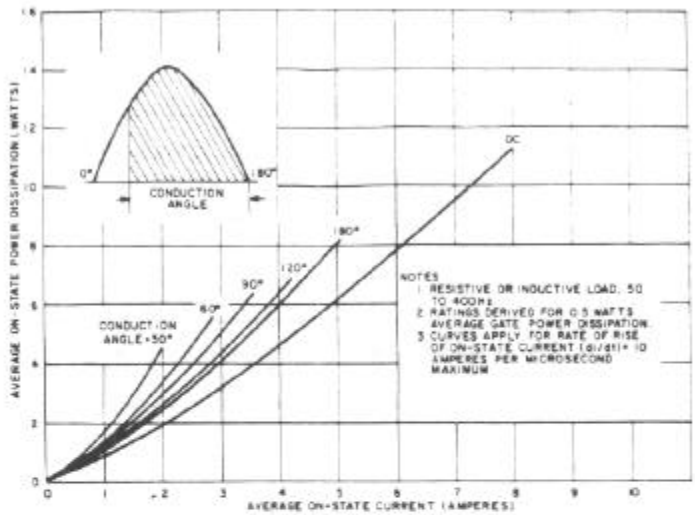
CHARACTERISTICS

Test	Symbol	Min.	Typ.	Max.	Units	Test Conditions
Peak Off-state or Reverse Current (1)	I_{DRM} or I_{RRM}				mA	$V_{DRM} = V_{RRM}$ = Max. allowable volts peak
		–	–	0.1		T_C = + 25°C
		–	–	0.5		T_C = +100°C
Peak-On-State Voltage	V_{TM}	–	–	1.83	Volts	T_C = +25°C, I_{TM} = 16A peak. 1 Millisecond wide pulse, Duty cycle ≤ 2%
Critical Rate of Rise of Off-State Voltage (Higher values may cause device switching)	dv/dt	10	50	–	Volts/μsec	T_C = +100°C, Rated V_{DRM} Gate Open Circuited, Linear Waveform
Circuit Commutated Turn-Off Time	t_q	–	50	–	μsec	T_C = +100°C, I_{TM} = 10 A peak, Rectangular current pulse, 40 μsec duration, Commutation rate = -5 A/μsec. Peak reverse voltage = Rated volts max. Reverse voltage at end of turn-off time interval 12 volts min. Repetition rate = 60 pps. Rate of rise of re-applied off-stage voltage (dv/dt) = 10 V/μsec. Off-state voltage = Rated V. Gate bias during turn-off time interval = 0 volts, 100 ohms.
D.C. Gate Trigger Current	I_{GT}	–	–	25		T_C = +25°C V_D = 6 Vdc R_L = 91 ohms
		–	–	40	mAdc	T_C = -40°C V_D = 6 Vdc R_L = 45 Ohms
D.C. Gate Trigger Voltage	V_{GT}	–	–	1.5		T_C = +25°C V_D = 6 Vdc R_L = 91 Ohms
		–	–	2.0	Vdc	T_C = -40°C V_D = 6 Vdc R_L = 45 ohms
		0.2	–	–		T_C = +100°C Rated V_{DRM} R_L = 1000 ohms
Holding Current	I_H				mAdc	Anode source voltage = 24 Vdc, Peak initiating on-state current = 0.5 A, 0.1 msec to 10 msec wide pulse, Gate trigger source = 7V, 20 ohms
		–	–	30		T_C = +25°C
		–	–	60		T_C = -40°C
Latching Current	I_L				mAdc	Main Terminal Source Voltage = 24 Vdc, Gate trigger source = 15V, 100 ohms, 50 μsec rise and fall times max.
		–	–	60		T_C = +25°C
		–	–	120		T_C = -40°C
Steady-State (2) Thermal Resistance					°C/Watt	
	$R\theta_{JC}$	–	–	1.8		Junction to Case
	$R\theta_{JA}$	–	–	75		Junction to Ambient

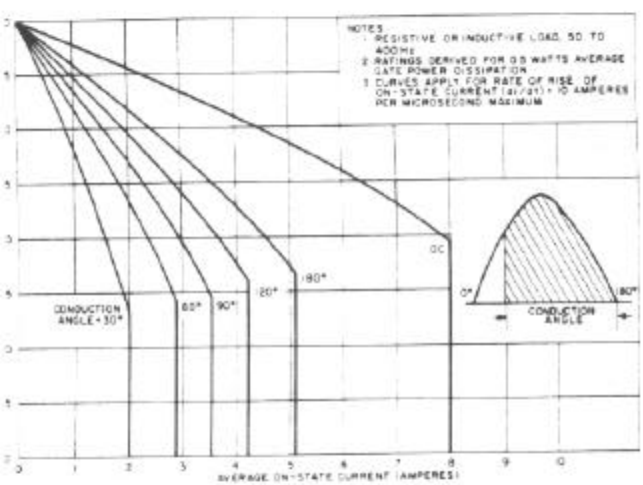
NOTES:
1. Values apply for zero or negative gate voltage only.
2. T_L is approximately equal to T_C, see outline drawing. The junction to ambient value is under worst case conditions, i.e., with #22 copper wire used for electrical contact to the terminals and natural convection.



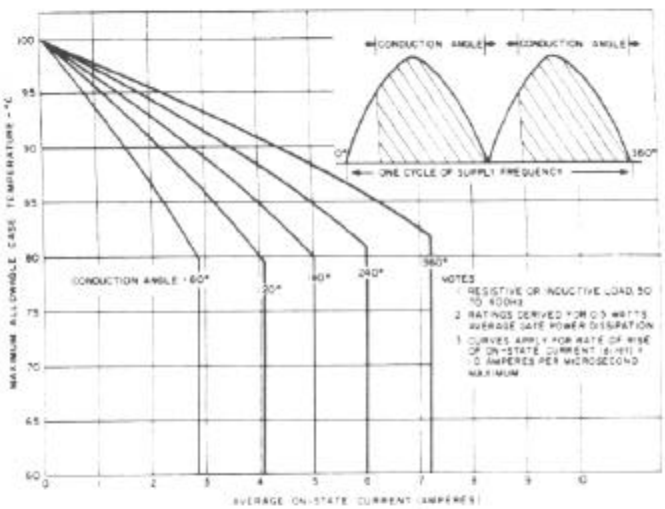
1. Max. On-State Voltage vs. On-State Current



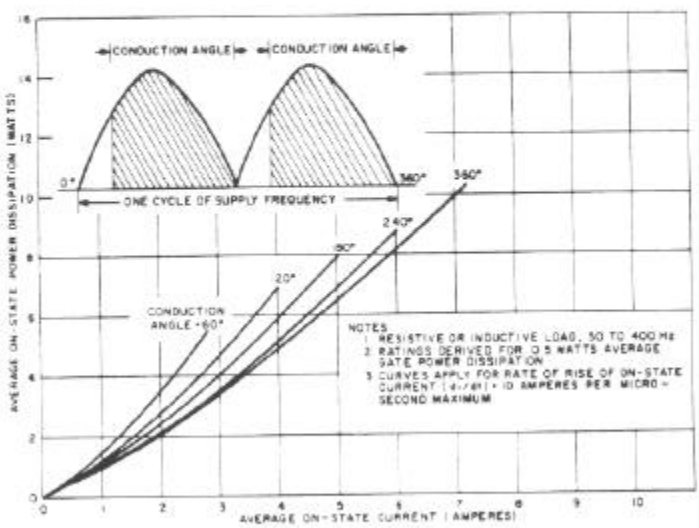
2. Max. On-State Power Dissipation for Half-Wave Rectified Sine Wave of Current



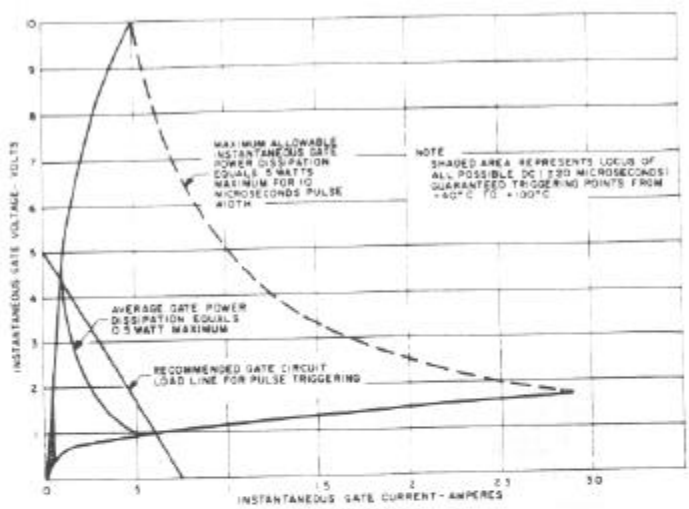
3. Max. Allowable Case Temperature For Half-Wave Rectified Sine Wave of Current


MAXIMUM ALLOWABLE CASE TEMPERATURE - °C
CONDUCTION ANGLE
CONDUCTION ANGLE
0°
360°
ONE CYCLE OF SUPPLY FREQUENCY
CONDUCTION ANGLE = 60°
360°
240°
120°
60°
NOTES
1. RESISTIVE OR INDUCTIVE LOAD, 50 TO 400Hz
2. RATINGS DERIVED FOR 0.5 WATTS AVERAGE GATE POWER DISSIPATION
3. CURVES APPLY FOR RATE OF RISE OF ON-STATE CURRENT (di/dt) = 10 AMPERES PER MICROSECOND MAXIMUM
AVERAGE ON-STATE CURRENT (AMPERES)

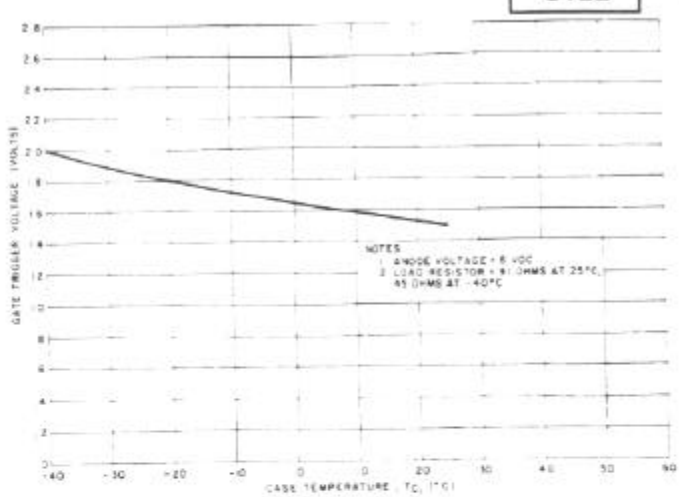
4. Max. Allowable Case Temperature For Full-Wave Rectified Sine Wave of Current


AVERAGE ON-STATE POWER DISSIPATION (WATTS)
CONDUCTION ANGLE
CONDUCTION ANGLE
0°
360°
ONE CYCLE OF SUPPLY FREQUENCY
360°
240°
120°
60°
CONDUCTION ANGLE = 60°
NOTES
1. RESISTIVE OR INDUCTIVE LOAD, 50 TO 400 Hz
2. RATINGS DERIVED FOR 0.5 WATTS AVERAGE GATE POWER DISSIPATION
3. CURVES APPLY FOR RATE OF RISE OF ON-STATE CURRENT (di/dt) = 10 AMPERES PER MICROSECOND MAXIMUM
AVERAGE ON-STATE CURRENT (AMPERES)

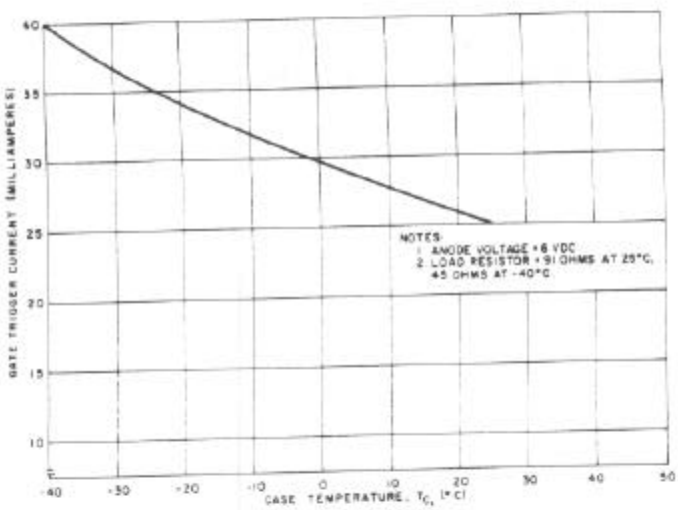
5. Max. Allowable On-State Power Dissipation for Full-Wave Sine Wave of Current


INSTANTANEOUS GATE VOLTAGE - VOLTS
INSTANTANEOUS GATE CURRENT - AMPERES
MAXIMUM ALLOWABLE INSTANTANEOUS GATE POWER DISSIPATION EQUALS 5 WATTS MAXIMUM FOR 10 MICROSECONDS PULSE WIDTH
AVERAGE GATE POWER DISSIPATION EQUALS 0.5 WATT MAXIMUM
RECOMMENDED GATE CIRCUIT LOAD LINE FOR PULSE TRIGGERING
NOTE
SHADED AREA REPRESENTS LOCUS OF ALL POSSIBLE DC (120 MICROSECONDS) GUARANTEED TRIGGERING POINTS FROM +60°C TO +130°C

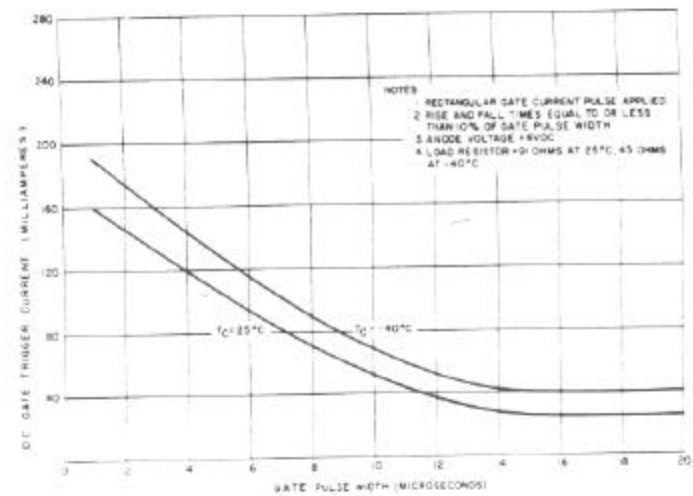
6. Gate Trigger Characteristics



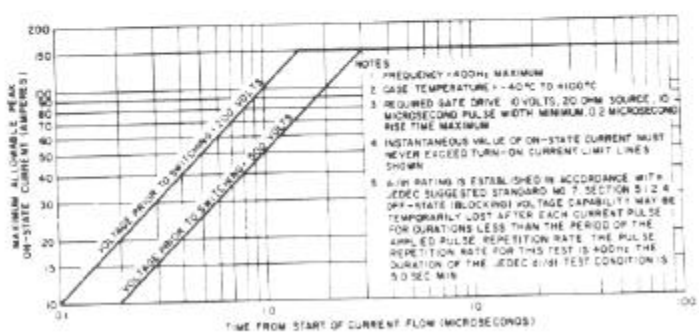
7. Max. DC Gate Voltage to Trigger vs. Case Temperature


GATE TRIGGER CURRENT (MILLIAMPERES)
CASE TEMPERATURE, T_C, (°C)
NOTES
1. ANODE VOLTAGE = 6 VDC
2. LOAD RESISTOR = 91 OHMS AT 25°C, 45 OHMS AT -40°C

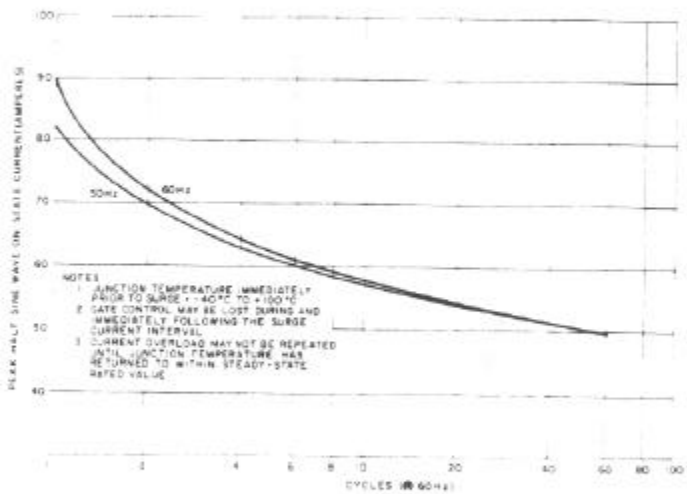
8. Max. DC Gate Current to Trigger vs. Case Temperature


DC GATE TRIGGER CURRENT (MILLIAMPERES)
GATE PULSE WIDTH (MICROSECONDS)
NOTES
1. RECTANGULAR GATE CURRENT PULSE APPLIED
2. RISE AND FALL TIMES EQUAL TO OR LESS THAN 10% OF GATE PULSE WIDTH
3. ANODE VOLTAGE = 6 VDC
4. LOAD RESISTOR = 91 OHMS AT 25°C, 45 OHMS AT -40°C
T_C = 25°C
T_C = -40°C

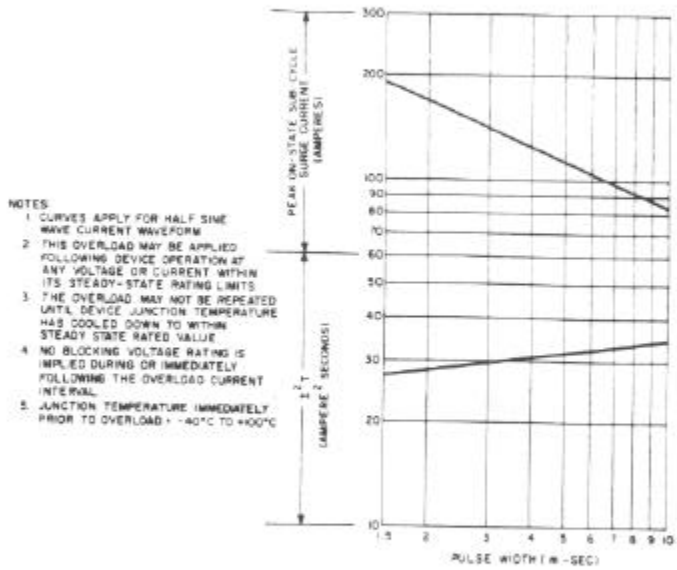
9. Max. DC Gate Current to Trigger vs. Gate Pulse Width


MAXIMUM ALLOWABLE PEAK ON-STATE CURRENT (AMPERES)
TIME FROM START OF CURRENT FLOW (MICROSECONDS)
NOTES
1. FREQUENCY = 400Hz MAXIMUM
2. CASE TEMPERATURE = -40°C TO +100°C
3. REQUIRED GATE DRIVE: 10 VOLTS, 20 OHM SOURCE, 10 MICROSECOND PULSE WIDTH MINIMUM, 0.2 MICROSECOND RISE TIME MAXIMUM
4. INSTANTANEOUS VALUE OF ON-STATE CURRENT MUST NEVER EXCEED TURN-ON CURRENT LIMIT LINES SHOWN
5. di/dt RATING IS ESTABLISHED IN ACCORDANCE WITH JEDEC SUGGESTED STANDARD NO 7, SECTION 5.1.2.4. OFF-STATE (BLOCKING) VOLTAGE CAPABILITY MAY BE TEMPORARILY LOST AFTER EACH CURRENT PULSE FOR DURATIONS LESS THAN THE PERIOD OF THE APPLIED PULSE REPETITION RATE. THE PULSE REPETITION RATE FOR THIS TEST IS 400Hz THE DURATION OF THE JEDEC di/dt TEST CONDITION IS 5.0 SEC MIN
200 VOLTS PRIOR TO SWITCHING 100 VOLTS
100 VOLTS PRIOR TO SWITCHING 200 VOLTS

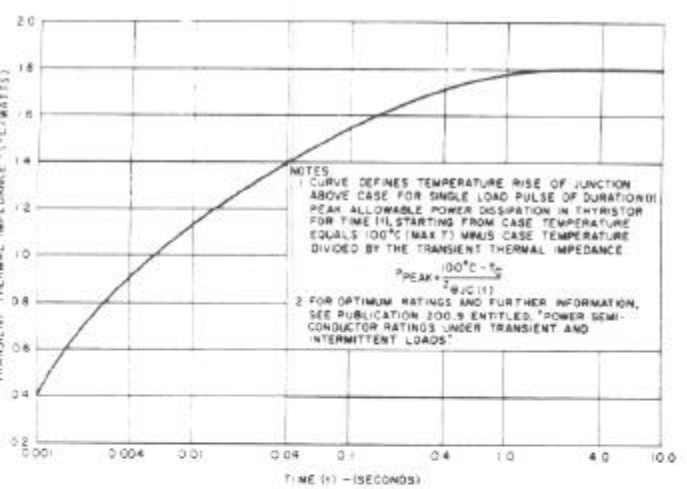
10. Turn-On Current Limit


PEAK HALF SINE WAVE ON STATE CURRENT (AMPERES)
50Hz
60Hz
NOTES
1. JUNCTION TEMPERATURE IMMEDIATELY PRIOR TO SURGE = -40°C TO +100°C
2. GATE CONTROL MAY BE LOST DURING AND IMMEDIATELY FOLLOWING THE SURGE CURRENT INTERVAL
3. CURRENT OVERLOAD MAY NOT BE REPEATED UNTIL JUNCTION TEMPERATURE HAS RETURNED TO WITHIN STEADY-STATE RATED VALUE
CYCLES (@ 60Hz)

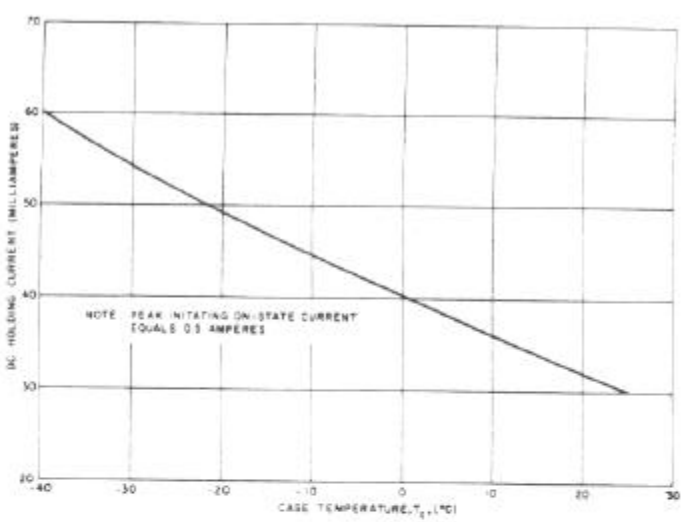
11. Max. Allowable Surge Current Following Rated Load Conditions


NOTES
1. CURVES APPLY FOR HALF SINE WAVE CURRENT WAVEFORM
2. THIS OVERLOAD MAY BE APPLIED FOLLOWING DEVICE OPERATION AT ANY VOLTAGE OR CURRENT WITHIN ITS STEADY-STATE RATING LIMITS
3. THE OVERLOAD MAY NOT BE REPEATED UNTIL DEVICE JUNCTION TEMPERATURE HAS COOLED DOWN TO WITHIN STEADY STATE RATED VALUE
4. NO BLOCKING VOLTAGE RATING IS IMPLIED DURING OR IMMEDIATELY FOLLOWING THE OVERLOAD CURRENT INTERVAL
5. JUNCTION TEMPERATURE IMMEDIATELY PRIOR TO OVERLOAD = -40°C TO +100°C
PEAK ON-STATE SUB-CYCLE SURGE CURRENT (AMPERES)
I^2t (AMPERE^2 SECONDS)
PULSE WIDTH (m-SEC)

12. Sub-cycle Surge and I^2t Rating Following Rated Load Conditions


NOTES
1. CURVE DEFINES TEMPERATURE RISE OF JUNCTION ABOVE CASE FOR SINGLE LOAD PULSE OF DURATION (t). PEAK ALLOWABLE POWER DISSIPATION IN THYRISTOR FOR TIME (t), STARTING FROM CASE TEMPERATURE EQUALS 100°C (MAX T_j) MINUS CASE TEMPERATURE DIVIDED BY THE TRANSIENT THERMAL IMPEDANCE
$P_{PEAK} = \frac{100°C - T_C}{Z_{\theta JC}(t)}$
2. FOR OPTIMUM RATINGS AND FURTHER INFORMATION, SEE PUBLICATION 200.9 ENTITLED, "POWER SEMICONDUCTOR RATINGS UNDER TRANSIENT AND INTERMITTENT LOADS"
TIME (t) - (SECONDS)

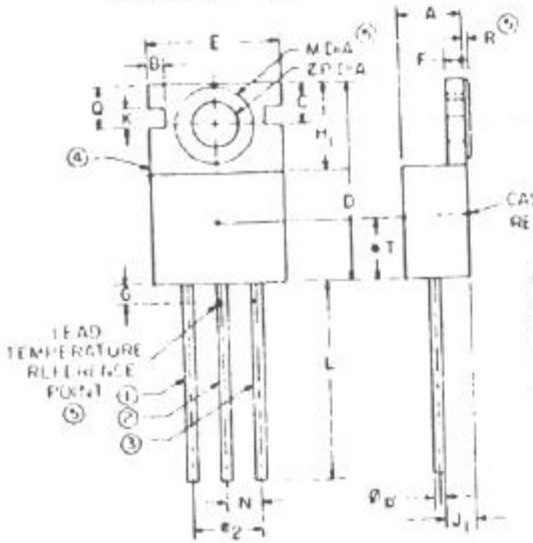
13. Max. Transient Thermal Impedance, Junction to Case



14. Max. DC Holding Current vs. Case Temperature

OUTLINE DRAWINGS

STANDARD TYPE



TYPE 1

① ANODE
② CATHODE
③ GATE
④ MOUNTING TAB ELECTRICALLY COMMON TO MT2. NON - ISOLATED DEVICES ONLY
⑤ NON - ISOLATED DEVICES ONLY

TERMINAL ARRANGEMENT

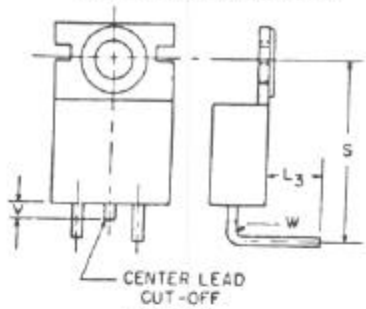
	INCHES	

TERMINAL ARRANGEMENT

SYMBOL	INCHES		METRIC MM	
	MIN	MAX	MIN	MAX
A	.160	.190	4.06	4.83
B	.054 TYP.		1.37 TYP.	
Ø b	.029	.035	.73	.89
C	.110	.120	2.79	3.05
D	.560	.650	14.23	16.51
E	.390	.420	9.90	10.67
θ_2	.190	.210	4.82	5.33
F	.040	.055	1.01	1.39
G	—	.065	—	1.65
H_1	.240	.260	6.09	6.60
J_1	.085	.115	2.15	2.92
K	.054 REF.		1.37 REF	
L	.500	—	12.70	—
L_3	.360	—	9.14	—
M	.232	.236	5.89	5.99

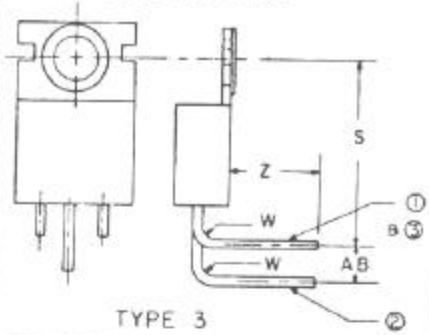
SYMBOL	INCHES		METRIC MM	
	MIN	MAX	MIN	MAX
N	.095	.105	2.41	2.67
Ø P	.141	.145	3.58	3.68
Q	.118 REF.		3.00 REF.	
R	0015	.004	—	.10
S	.570	.590	14.47	14.99
T	—	.220	—	5.59
V	.040	.070	1.01	1.78
W	.020	.030	.50	.76
Z	.172	.202	4.36	5.13
AA	.087	.097	2.20	2.46
AB	.120	.130	3.04	3.30
AC	.025	.035	.63	.89
AD	.045	.055	1.14	1.40
AE	.353	.433	8.96	11.00

TO-66 EQUIVALENT
(NON-ISOLATED DEVICES ONLY)



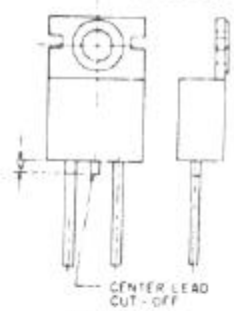
TYPE 2

FLAT MOUNTING
CHASSIS HEATSINK



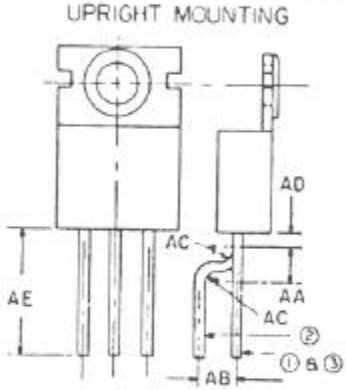
TYPE 3

CENTER LEAD CUT
(NON-ISOLATED DEVICES ONLY)



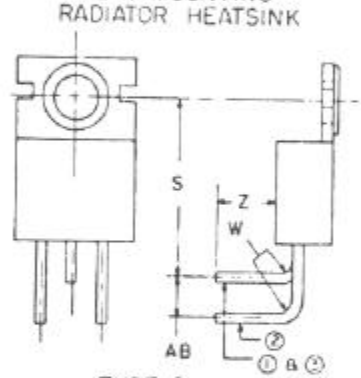
TYPE 4

UPRIGHT MOUNTING



TYPE 5

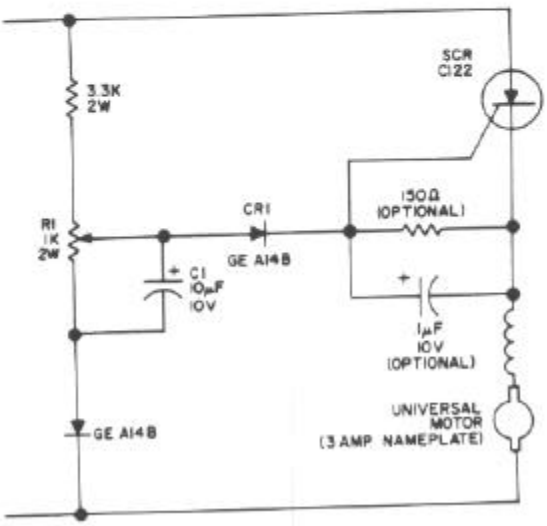
FLAT MOUNTING
RADIATOR HEATSINK



TYPE 6

C122

TYPICAL CIRCUIT



This circuit uses the counter EMF of the motor armature due to residual field as a feedback signal of motor speed to maintain essentially constant speed characteristics with varying torque requirements. There will be some variation in the effectiveness of speed control from one motor to another depending on the magnitude of the residual field for the particular motor.

During the positive half cycle of the supply voltage, a reference voltage is established on the arm of the potentiometer R_1 which is compared with the counter EMF of the motor through the gate of the SCR. When the "pot" voltage rises above the counter EMF, current flows through CR_1 into the gate of the SCR, and thus applying the remainder of that half cycle of supply voltage to the motor. If load is applied to the motor, its speed tends to decrease, thus decreasing counter EMF in proportion to speed. The "pot" reference voltage thus causes current to flow into the SCR gate earlier in the cycle. The SCR triggers earlier in the cycle, and additional voltage is applied to the armature to compensate for the increased load and to maintain the preset speed. The particular speed at which the motor operates can be selected by R_1. Stable operation is possible over approximately a 10 to 1 speed range. Stability at very low speeds can be improved by reducing the value of C_1 at the expense of feedback gain.

OTHER APPLICATION NOTES OF INTEREST

Publication Number	Application Notes
200.31	Phase Control of SCR's With Transformer and Other Inductive AC Loads
200.33	Regulated Battery Charges Using the Silicon Controlled Rectifier
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